



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,579	10/23/2003	Noriyuki Miura	MAE 296	5973
23995	7590	10/04/2006	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			FARAHANI, DANA	
			ART UNIT	PAPER NUMBER
			2891	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/690,579	Applicant(s) MIURA, NORIYUKI	
	Examiner Dana Farahani	Art Unit 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-6,8,9,11-14 and 16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-6,8,9,11-14 and 16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3-6, 8, 9, 11-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al., hereinafter Okada (US Patent 6,093,243), newly cited.

As for claims 1, 3, 8, 9, 11 and 16, Okada discloses figure(s) 148 a semiconductor substrate 1001;

a gate insulator; and

a gate electrode 1007a disposed on said gate insulator;

wherein a source, a drain, and a channel are formed, thereby forming a MOSFET; also disclosing channel length of 0.25 Microns with the concentration of 6×10^{17} (see col. 71, lines 24-37).

Okada does not disclose in the embodiment, an SOI type FET, and that said gate electrode is made of P-type and conductivity types of said source, said drain, and said channel are all N-type, rather discloses the impurity types are the other way around. Okada discloses an SOI type FET of figure 78. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the FET of the embodiment of figure 148 as an SOI type to benefit from the properties associated with SOI FETs such as better device insulation, and to flip the conductivity types in the device, since they are recognized to be equivalent, and one of

Art Unit: 2891

ordinary skill in the art can choose a desirable conductivity type to be able to choose the material and process available at the manufacturing step of the device.

As for claims 4-6 and 12-14, Okada discloses the limitations in the claims, except for the range of thickness of the gate insulator is between approximately 1 to 4 nm, or more specifically 2nm, and that of the SOI film is from 10-40 nm, and the impurity concentration of source and drain is no less than approximately 1×10^{21} . However, the gate thickness of Okada is also in less than 10 nm range, and forming a 50 nm silicon layer 1005b on said oxide layer is feasible (col. 69, lines 44 and subseq), evidencing that forming the SOI layer and the gate insulator layer as thin as what is claimed is feasible. It would have been obvious to one of ordinary skill in the art to adjust the thickness of the gate insulator to be this small in order to achieve a desirable threshold voltage, and the thickness of the gate insulator of the reference and that of claimed differ negligibly; and it would have been obvious to make the thickness of the SIO film as small to confine the channel current even more; and also make the source and drain as high impurity regions, in order to omit a step of forming source and drain contacts, such that external contacts can be made directly to source and drain, since they will have low contact resistance due to the high concentration.

Response to Arguments

3. Applicant's arguments, see the response, filed 10/18/05, with respect to the previously rejected claims have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as set forth above.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DF



**B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER**